

## Anomalous L2 rejections

- Symptoms of the problem:
  - where and how was it found?
  - trigger mask data path
- Data integrity
  - L2 software/hardware checks
  - further cross checks
- Future (new) monitoring
- Data quality and conclusions





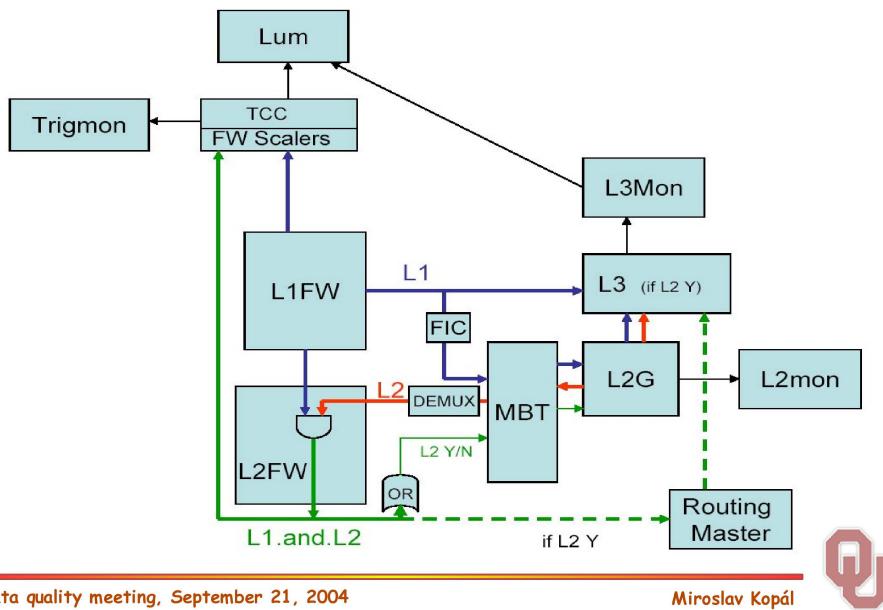
#### L1/L2 bit mask

- When was the problem found?
  - when v13 was put on-line:
    - bit 009 with L2 rejection ~26 when it only 2-3 was expected
    - bit 057 with L2 rejection 2.4 when 1.0 was expected (no L2 conditions)
  - 1<sup>st</sup> "bad" run: 192823, 1<sup>st</sup> "good" run: 194598
- Where was it found?
  - run luminosity reports (not only v13, but when older luminosity reports were checked, this problem has been around for a while in v12, too)
  - Trigger Meisters: daqdialog/12mon
  - BUT all three programs look at the <u>SAME</u> numbers (L1 scalers)
    so they did not give us any new information





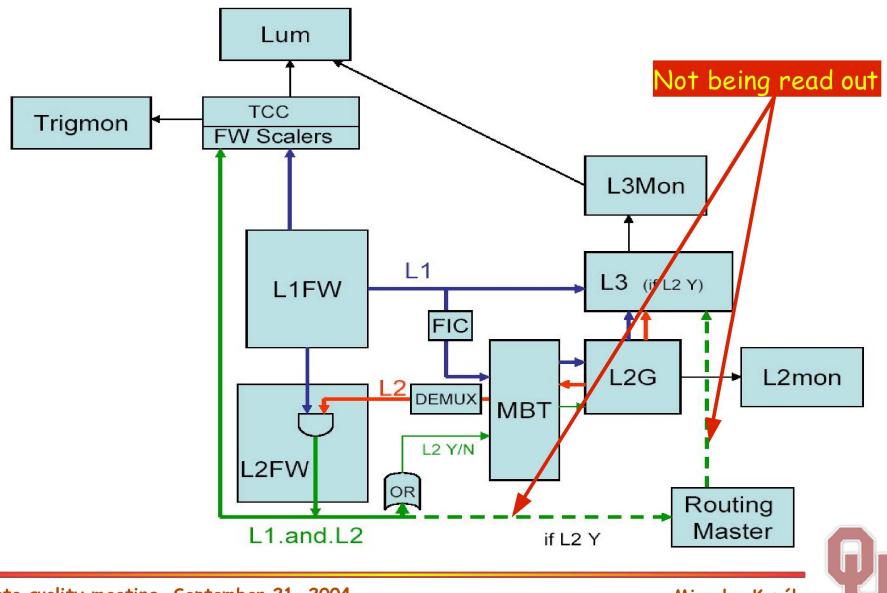
## Bit mask - path





## Bit mask - path

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### Bit mask - monitoring

- Problem appeared on May 9, when L2GBL's pilot MBT was replaced due to its malfunctioning (trigger v12)
- On June 29, this MBT was replaced
  - how could we monitor/recognize it?
    - check the luminosity reports rather off-line monitoring created one-two days after the run was taken
    - or, stare at the 12mon screen
    - or, monitor triggers with no L2 restrictions ⇒ trigstripmon but must know which ones and must know the base line - this is on-line monitoring



## L2 faulty MBT

6

#### MBT - hardware:

- 128 bit L2 answer comes out of the MBT in eight 16 bit words (sent out sequentially from the same driver)
- MBT bit 9 of 16 broken differential pair 6 M $\Omega$  instead of expected 130  $\Omega$  to ground affects L2 answer bits 9, 25, 41, 57, 73, 89 and 105
- Results: sometimes reports "reject" (FALSE) instead of "accept" (TRUE) it seems that this happens when the neighboring bit is set to TRUE (logic levels are inverted)
- = faulty MBT

Output goes ONLY to HWFW and luminosity scalers, but NOT to L3





### L2 software

#### • L2 code:

- "OR" of all L2 trigger bits must agree with L1 TFW
- disagreement would raise an error, stop the data flow and request SCL-init
  - this is fully automated daqAI
  - it could be unnoticed if it happens "frequently", DAQ shifter would notice and alarm L2 experts
  - going through all L2 log files, this happened only 2 times between May 9 and June 28/29
- This check was/is/will be working before/during/after the incident
- L2 GBL bits written to tape are NOT affected by the MBT



# ymptoms (from lumi reports)

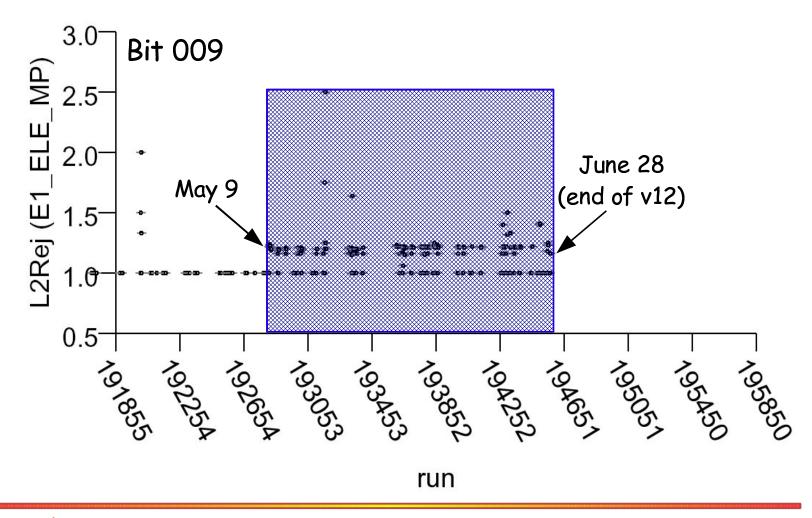
- Luminosity reports give L3 trigger names
- Total of 308 runs with this hardware configuration (+ 24 runs when L3 trigger names were on L1 bits 10, 26, etc. ...)

bit #	L1 name	L3 name			
009	CEM(1,11)_ncu^2	E1_ELE_MP, E1_SHT20, E1_SH30, E1_L50, E1_VL70, E1_SHT15_M15, E1_L20_M25, E1_SHT15_TK13, E1_T7SHT8_2TK5, E1_T7SHT8_M10, E1_T13L15, E1_T25VL30, E1_2L20, E1_2SH8, E1_2L15_SH15, E1_2L8_T8L8, E1_SHT15_2J20, E1_SH15_2J20_M10, E1_SHT15_2J_HT50			
025	CJT(3,5)_ncu^4	MHT20_L2L0_PVZ			
041	mu1ptxwtxx_ncu^2	MU_W_L2M3_L3L15 (?)			
057	mu1pt4wlxx_CJT(1,3)_ncu	never fired			
073	mu2ptxatxx_ncu	mu2ptxatxx			
089	mu2ptxcllxmu1ptxctlx_ncu^3	2MU_C_2L2_2TRK			
105	ALMSouth[v]ALMNorth[v]_ncu	zero_bias_GapSN_NCU			



# Symptoms (from lumi reports)

What do we see from luminosity reports?





Bit 025

194651

194252

193852

193453

<sub>193053</sub>

192654

192254

191855

10.

0.0

run

Bit 073

1.12

1.04

L2Rej (mu2ptxatxx)

0.88

-96.0

-8.0

+**!!**|

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193951

193652

193352

193053

192753

192454

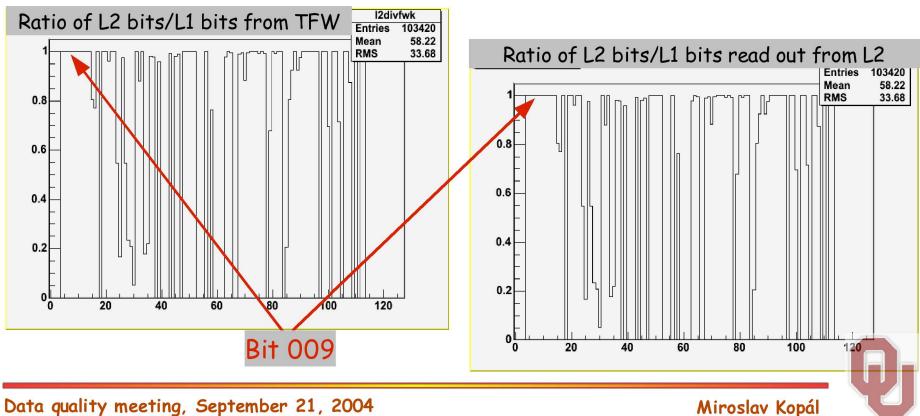
192154

191855

run

## Cross check of L1/L2 masks on tape

- Check the trigger masks off-line using the monitor stream (and also all data stream)
- If there was extra L2 rejection, it should be observed (run 192823, by Bob Hirosky)





#### • Test № 1:

- test single bits use zero\_bias triggers on each bit, firing at L2 with
  50% probability
- bit 9 of the bad MBT behaved normally, no extra L2 rejection was observed

#### • Test № 2:

- if L1TWF "OR" does not agree with L2 "OR", L2 must complain
- Dan Edmunds set an L1TWF bit off after L2 received the trigger mask  $\Rightarrow$  L2 reacted correctly  $\Rightarrow$  L2 raised an error and requested SCL-init
- this worked with both, bad and good, MBTs as expected
- No L2 software changes during this period of time!
- Bit mask consistency check works ⇒ L2 monitoring seen in the luminosity reports is wrong



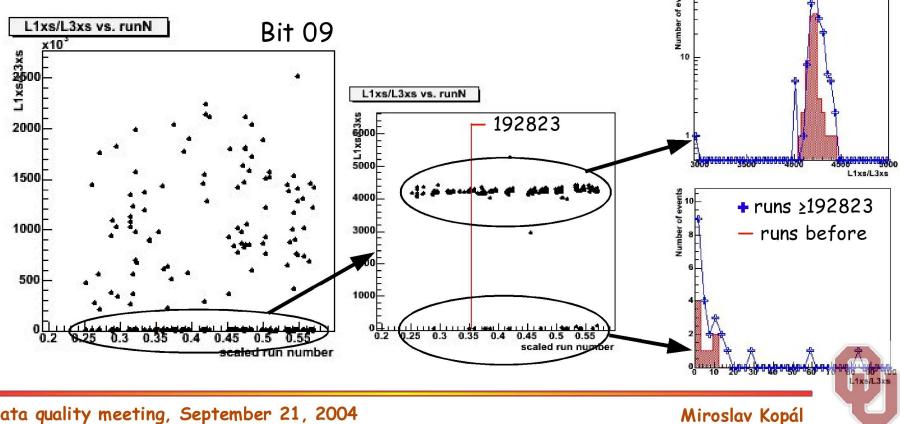


### More cross checks ...

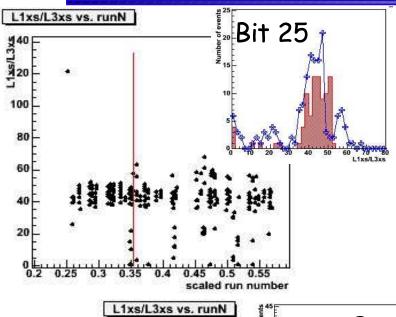
Using luminosity report data, we looked at L1xs/L3xs ratio and L1xs/L2xs ratio

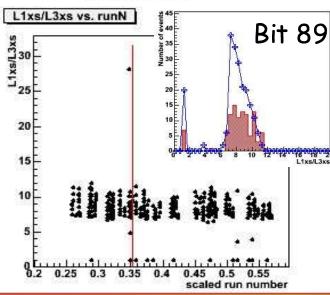
No difference has been observed in runs taken before and after

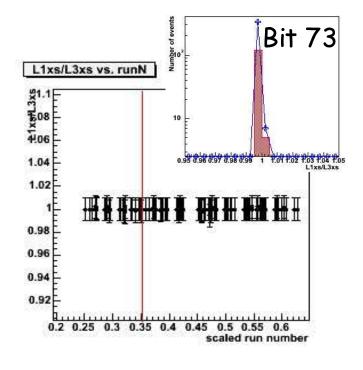
May 9 (run 192823):



## More cross checks (xs: L1/L3)

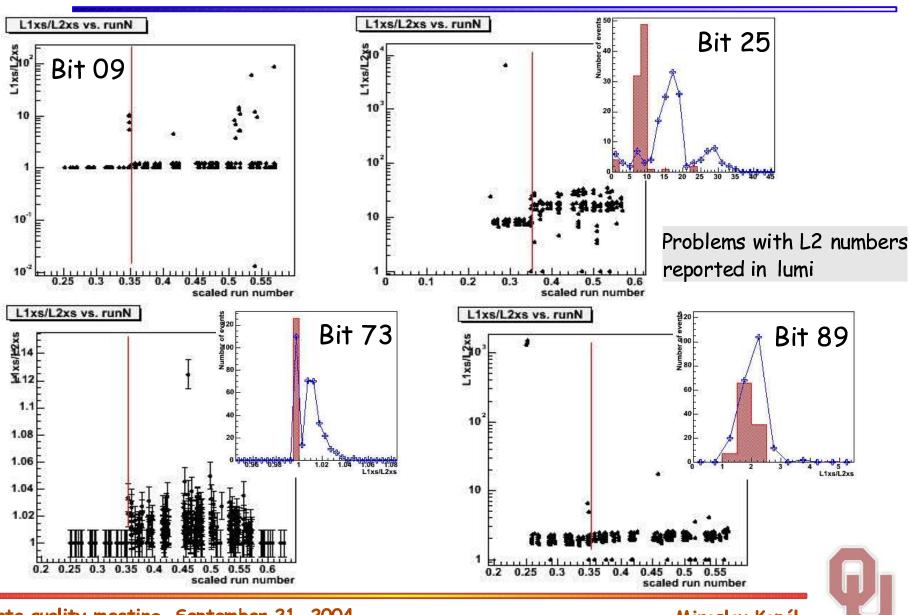






No problems with L3 numbers reported in lumi







## Future (new) monitoring

- L3 monitoring crate compare L2 trigger masks:
  - compare L1 x L2 (green) with L1 x L3 (red x blue)
    from L2 GBL in L3
  - compare L1 (blue from L1) with L1 (blue from L2
    GBL) in L3





### Conclusions

- Problem was observed in at least two different places:
  - luminosity reports
  - 12mon/daqdialog
- Both monitors are based on the same L1 scaler numbers
- Faulty MBT current model only bit 9 has wrong resistance but failure appears based on cross talk within the bit mask
- This problem does not make luminosity blocks bad





#### L2 decisions are correct!

- If "OR" of L2 bit mask does not agree with "OR" of TWF bit mask, L2 raises an error - this check is working and does not fail
- L2 and L3 decisions are unaffected by this L2 problem
  - check with luminosity scalers for L1 and L3 X5 and there is no change!
- Data quality
  - no discontinuity at L3, no problems with the data ⇒ data is all
    GOOD!
  - the only precaution must be taken when studying L2 trigger efficiencies for affected bits - change in DB
  - L2 mask on tape is correct (because MBT is out of the path)



#### More cross checks ...

#### What was the unique rate?

(rate of a group of triggers when all other triggers do not fire)

- trigger configuration was such as to prevent bits 9, 25, ... from being the only triggers which fired at L2
- however, L3 triggers grouped to L2 bits do have a unique rates
- **no difference** for bits 9, 25, ... in L3 trigger group rates before and after May 9

Trigger Name	# of events	s bandwidth fraction	rate to tape (Hz)	unique fraction	unique rate to tape (Hz)	largest overlap with trigger	largest overlap
Group_L2bit105	174	0.000	0.017	1.000	0.02	none	0.000
Group_L2bit089	10585	0.029	1.044	0.503	0.53	MUW_L2M0_2TK3_MM	0.231
Group_L2bit073	999	0.003	0.098	0.565	0.06	2MU_A_L2M0	0.428
Group_L2bit041	9178	0.025	0.905	0.010	0.01	MUW_W_L2M3_TRK10	0.961
Group_L2bit025	14514	0.039	1.431	0.570	0.82	MHT30_3CJT5	0.172
Group_L2bit009	44288	0.119	4.366	0.169	0.74	E3_SHT20	0.322

